IN THE CLAIMS:

1. (Currently Amended) A parallel execution processor comprising:

a plurality of processing elements;

an obtaining unit operable to obtain an instruction sequence including one or more instructions;

a decoding unit operable to decode the obtained instruction sequence into the one or more instructions;

a group forming unit operable to form the processing elements into as many groups as the number of instructions included in the instruction sequence; ~~and~~

a plurality of register files, each of which corresponds to a different one of the processing elements; and

an execution controlling unit operable to assign the one or more instructions decoded by the decoding unit to the groups of the processing elements, so that each group of the processing elements receives a different one of the one or more instructions, and control the processing elements so that (i) the instructions received by the groups of the processing elements are executed in parallel, ~~and~~ (ii) in each group, all processing elements in the group each execute the same instruction received by the group, and (iii) each processing element receives data from a different register file.

2. (Cancelled)

3. (Previously Presented) The parallel execution processor of Claim 1, wherein

when the number of instructions included in the instruction sequence is one, the group forming unit forms all of the processing elements into one group, and

when the number of instructions included in the instruction sequence is two, the group forming unit forms all of the processing elements into two groups so that the two groups contain an equal number of processing elements.

4. (Currently Amended) The parallel execution processor of Claim 3, ~~further comprising~~

~~a plurality of register files, each of which corresponds to a different one of the processing elements,~~ wherein

the instruction sequence includes a first instruction and a second instruction,

the register files are arranged in the register so that first-group register files and second-group register files alternate, (i) the first-group register files each storing therein a piece of data to be processed when the first instruction is executed and (ii) the second-group register files each storing therein a piece of data to be processed when the second instruction is executed,

when the number of instructions included in the instruction sequence is two, the group forming unit forms the processing elements corresponding to the first-group register files into one of the two groups, and the processing elements corresponding to the second-group register files into the other group, and

each of the processing elements obtains the piece of data to be processed from the corresponding register file.

5. (Previously Presented) The parallel execution processor of Claim 4, wherein

the register files are formed into a plurality of pairs, keeping an order in which the register files are arranged,

each of the instructions includes a piece of selection information indicating which piece of data each processing element should obtain, selecting out of (a) the piece of data stored

in the corresponding register file and (b) the piece of data stored in a register file with which the corresponding register file is paired, and

each of the processing elements obtains the piece of data to be processed from the register file indicated in each piece of selection information.

6. (Previously Presented) The parallel execution processor of Claim 3, wherein

when the number of instructions included in the instruction sequence is two, the execution controlling unit includes:

a storing unit that stores therein a plurality of combination options based on which of the processing elements should belong to each of the two groups, the combination options being prepared for each of a plurality of grouping procedures;

a grouping information obtaining unit operable to obtain a piece of grouping information indicating which one of the grouping procedures should be used; and

a selecting unit operable to select one of the combination options according to the obtained piece of grouping information.

7. (Previously Presented) The parallel execution processor of Claim 3, wherein

when the number of instructions included in the instruction sequence is two, the execution controlling unit includes:

a grouping information obtaining unit operable to obtain a piece of grouping information indicating to which one of the two groups each of the processing elements should belong; and

a grouping unit operable to form the processing elements into the two groups according to the obtained piece of grouping information.

8. (Previously Presented) The parallel execution processor of Claim 1, further comprising

a fetching unit operable to fetch a piece of data which is of a predetermined length and has a format field and a data field, wherein

each of the instructions includes an OP code and an operand,

a positioning pattern is written in the format field, the positioning pattern being for positioning OP codes and operands in the data field,

in the piece of data, one or more OP codes and one or more operands are arranged in the data field in an order defined by the positioning pattern written in the format field,

the obtaining unit obtains, as the instruction sequence, the piece of data of the predetermined length fetched by the fetching unit,

the decoding unit extracts, from the piece of data, the one or more OP codes and the one or more operands, according to the positioning pattern so as to decode the OP codes and the operands of the instructions, and

the execution controlling unit assigns, in the defined order, the decoded instructions to the groups.

9. (Previously Presented) The parallel execution processor of Claim 1, further comprising:

a fetching unit operable to fetch a piece of data which is of a predetermined length; and

a storing unit operable to store therein a predetermined positioning pattern for OP codes and operands, wherein

each of the instructions includes an OP code and an operand,

one or more OP codes and one or more operands are arranged in the piece of data in an order defined by the predetermined positioning pattern,

the obtaining unit obtains, as the instruction sequence, the piece of data of the predetermined length fetched by the fetching unit

the decoding unit extracts, from the piece of data, the one or more OP codes and the one or more operands, according to the positioning pattern stored in the storing unit so as to decode the OP codes and the operands of the instructions, and

the execution controlling unit assigns, in the defined order, the decoded instructions to the groups.

10. (Previously Presented) The parallel execution processor of Claim 1, wherein

when the instruction sequence obtained by the obtaining unit includes two or more instructions and one of the instructions instructs that processing elements included in some of the groups should halt operation, the execution controlling unit controls the processing elements included in those groups so that those processing elements halt operation.

11.-13. (Cancelled)

14. (Currently Amended) An instruction assigning method for assigning instructions to a plurality of processing elements for executing in parallel one instruction to be assigned to one group of the processing elements, comprising:

an obtaining step of obtaining an instruction sequence including one or more instructions;

a decoding step of decoding the obtained instruction sequence into the one or more instructions;

a group forming step of forming the processing elements into as many groups as the number of instructions included in the instruction sequence; and

an execution controlling step of assigning the one or more instructions decoded in the decoding step to the groups of the processing elements, so that each group of the processing elements receives a different one of the one or more instructions, and controlling the processing elements so that (i) the instructions received by the groups of the processing elements are executed in parallel, ~~and~~ (ii) in each group, all processing elements in the group each execute in parallel the same instruction received by the group, and (iii) each processing element receives data from a different register file.

15. (Cancelled)

16. (Currently Amended) A parallel execution processor system for processing a plurality of instruction sequences comprising:

a plurality of processing elements;

an obtaining unit for obtaining an instruction sequence including one or more instructions, wherein the number of processing elements is greater than the number of instructions;

a decoding unit for decoding the obtained instruction sequence into the one or more instructions;

a group forming unit for forming the processing elements into as many groups as the number of instructions included in the instruction sequence; ~~and~~

a plurality of register files, each of which corresponds to a different one of the processing elements; and

an execution controlling unit for assigning the one or more instructions decoded by the decoding unit to the groups of the processing elements, so that each group of the processing elements receives a different one of the one or more instructions, and control the processing elements so that (i) the instructions received by the groups of the processing elements are executed in parallel, ~~and~~ (ii) in each group, all processing elements in the group each execute in parallel the same instruction received by the group, and (iii) each processing element receives data from a different register file.

17. (Previously Presented) The parallel execution processor system of Claim 16 further comprising at least two processing elements and wherein the obtaining unit obtains an instruction sequence including only one instruction.

18. (Previously Presented) The parallel execution processor system of Claim 16 further including a source of a plurality of instructions.

19. (Previously Presented) The parallel execution processor system of Claim 18 further comprising at least four processing elements and wherein the obtaining unit obtains an instruction sequence including a maximum of two instructions.

20. (Previously Presented) The parallel execution processor system of Claim 18 further comprising at least 64 processing elements and wherein the obtaining unit obtains an instruction sequence including a maximum of 32 instructions.

21. (Previously Presented) The parallel execution processor system of Claim 18 further comprising at least 128 processing elements and wherein the obtaining unit obtains an instruction sequence including a maximum of 64 instructions.